

1 1. An adder circuit for adding a first binary number
2 and a second binary number, the adder comprising:
3 a carry evaluating circuit generating a carry
4 production control signal representing a sum of a block of
5 corresponding bits of the first binary number and the
6 second binary number and an input carry value to the block,
7 the carry production control signal comprising two signals
8 A and B that can each have a value of either P or Q; and
9 a conversion circuit coupled to receive the A and
10 B outputs and the conversion circuit outputting two signals
11 X and Y, each having a value of either P or Q, and X and Y
12 having one of three possible values.

1 2. An adder as in claim 1 wherein X and Y have one
2 of three possible values in accordance with:

| | | | |
|---|---------|----------|----------|
| 3 | | <u>X</u> | <u>Y</u> |
| 4 | Value 1 | P | P |
| 5 | Value 2 | Q | P |
| 6 | Value 3 | Q | Q. |

1 3. An adder as in claim 1 wherein X and Y have one
2 of three possible values in accordance with:

| | | | |
|---|---------|----------|----------|
| 3 | | <u>X</u> | <u>Y</u> |
| 4 | Value 1 | P | P |
| 5 | Value 2 | P | Q |
| 6 | Value 3 | Q | Q. |

1 4. An adder as in claim 1 wherein $P=0$ and $Q=1$.

1 5. An adder as in claim 1 further comprising:
2 a second circuit coupled to receive the X and Y
3 outputs and outputting a first result if the input carry
4 has a value of 1 and a second result if the input carry has
5 a value of 0.

1 6. An adder circuit as in claim 1 wherein the carry
2 evaluating circuit is coupled to two pairs of input signals
3 (A_1, b_1) and (A_2, b_2) that comprise one of two respective
4 pairs of bits of the first binary number and the second
5 binary number and two previously evaluated carry production
6 signals.

1 7. An adder circuit as in claim 1 wherein the carry
2 evaluating circuit is coupled to three pairs of input
3 signals (A_1, b_1) , (A_2, b_2) and (A_3, b_3) that comprise one of
4 three respective pairs of bits of the first binary number
5 and the second binary number and three previously evaluated
6 carry production signals.

1 8. An adder circuit as in claim 1 wherein the carry
2 evaluating circuit is coupled to four pairs of input
3 signals (A_1, b_1) , (A_2, b_2) , (A_3, b_3) and (A_4, b_4) that
4 comprise one of four respective pairs of bits of the first

5 binary number and the second binary number and four
6 previously evaluated carry production signals.

1 9. An adder circuit as in claim 1 wherein the carry
2 evaluating circuit is coupled to N pairs of input signals
3 (A_1, b_1) , (A_2, b_2) , (A_3, b_3) , (A_4, b_4) and (A_n, b_n) that
4 comprise one of N respective pairs of bits of the first
5 binary number and the second binary number and N previously
6 evaluated carry production signals.

1 10. An adder circuit as in claim 1 wherein a
2 plurality of carry evaluating circuits are used in a
3 parallel prefix structure to evaluate a full set of carry
4 bits from the first binary number and the second binary
5 number.

1 11. An adder as in claim 1, wherein the carry
2 evaluating circuit is formed of a plurality of static CMOS
3 logic gates.

1 12. An adder as in claim 1, wherein the carry
2 evaluating circuit is formed of a plurality of dynamic CMOS
3 logic gates.

1 13. An adder as in claim 1, further comprising:
 2 a carry binary number determining circuit,
 3 responsive to the first binary number and the second binary
 4 number and generating a carry binary number composed of
 5 carry bits of a sum of the first binary number and the
 6 second binary number, the carry binary number determining
 7 circuit having a plurality of circuit stages operating in
 8 series to generate the carry binary number, each circuit
 9 stage serving to partially resolve the carry binary number
 10 and at least one circuit stage including at least one of
 11 the carry bit evaluating circuits generating a carry
 12 control production signal that is coupled between the
 13 circuit stages as an input signal to a next circuit stage;
 14 and
 15 a combinatorial logic circuit coupled to
 16 respective corresponding bits of the first binary number,
 17 the second binary number and the carry binary number to
 18 generate a corresponding bit of a result binary number.

1 14. An adder as in claim 13, wherein the first,
 2 second and carry binary numbers have corresponding bits B1,
 3 B2, and B3 respectively, the combinatorial logic circuit
 4 performs a logical XOR operation on the three bits.

1 15. An adder as in claim 1, wherein the carry
 2 evaluating circuit is coupled to a microprocessor.

1 16. An adder as in claim 5, wherein the carry
2 evaluating circuit is coupled to a carry-select circuit.

1 17. A microprocessor comprising:
2 an arithmetic logic circuit including an adder
3 having a carry evaluating circuit generating a carry
4 production control signal representing a sum of a block of
5 corresponding bits of the first binary number and the
6 second binary number and an input carry value to the block,
7 the carry production control signal comprising two signals
8 A and B that can each have a value of either P or Q; and
9 a conversion circuit coupled to receive the A and B
10 outputs and the conversion circuit outputting two signals X
11 and Y, each having a value of either P or Q, and X and Y
12 having one of three possible values.

1 18. A microprocessor as in claim 17 further
2 comprising:
3 a second circuit coupled to receive the X and Y
4 outputs and outputting a first result if the input carry
5 has a value of 1 and a second result if the input carry has
6 a value of 0.

1 19. A microprocessor circuit as in claim 17 wherein
2 the carry evaluating circuit is coupled to two pairs of
3 input signals (A_1 , b_1) and (A_2 , b_2) that comprise one of two

4 respective pairs of bits of the first binary number and the
5 second binary number and two previously evaluated carry
6 production signals.

1 20. A microprocessor circuit as in claim 17 wherein
2 the carry evaluating circuit is coupled to three pairs of
3 input signals (A_1, b_1) , (A_2, b_2) and (A_3, b_3) that comprise
4 one of three respective pairs of bits of the first binary
5 number and the second binary number and three previously
6 evaluated carry production signals.

1 21. A microprocessor circuit as in claim 17 wherein
2 the carry evaluating circuit is coupled to N pairs of input
3 signals (A_1, b_1) , (A_2, b_2) , (A_3, b_3) , (A_4, b_4) and (A_n, b_n)
4 that comprise one of N respective pairs of bits of the
5 first binary number and the second binary number and N
6 previously evaluated carry production signals.

1 22. A microprocessor circuit as in claim 17 wherein a
2 plurality of carry evaluating circuits are used in a
3 parallel prefix structure to evaluate a full set of carry
4 bits from the first binary number and the second binary
5 number.

1 23. A microprocessor as in claim 17, further
 2 comprising:
 3 a carry binary number determining circuit,
 4 responsive to the first binary number and the second binary
 5 number and generating a carry binary number composed of
 6 carry bits of a sum of the first binary number and the
 7 second binary number, the carry binary number determining
 8 circuit having a plurality of circuit stages operating in
 9 series to generate the carry binary number, each circuit
 10 stage serving to partially resolve the carry binary number
 11 and at least one circuit stage including at least one of
 12 the carry bit evaluating circuits generating a carry
 13 control production signal that is passed between the
 14 circuit stages as an input signal to a next circuit stage;
 15 and
 16 a combinatorial logic circuit responsive to
 17 respective corresponding bits of the first binary number,
 18 the second binary number and the carry binary number to
 19 generate a corresponding bit of a result binary number.

1 24. A microprocessor as in claim 23, wherein the
 2 first, second and carry binary numbers have corresponding
 3 bits B1, B2, and B3 respectively, the combinatorial logic
 4 circuit performs a logical XOR operation on the three bits.

1 25. A microprocessor as in claim 23, wherein the
2 carry evaluating circuit is coupled to a carry-select
3 circuit.

1 26. A method for adding a first and a second binary
2 number, each having a plurality of bits, comprising:
3 generating a carry production control signal
4 representing a sum of a plurality of corresponding bits of
5 the first binary number and the second binary number and an
6 input carry value to the plurality of bits where the carry
7 production control signal comprises two signals A and B
8 that can each have a value of either P or Q; and
9 converting the A and B signals into two signals,
10 X and Y, representing one of three possible values.

1 27. The method of claim 26 further comprising:
2 receiving the X and Y signals and generating a
3 first result if the input carry has a value of 1 and a
4 second result if the input carry has a value of 0.

1 28. The method of claim 27 further comprising:
2 receiving the X and Y signals and generating a
3 final result utilizing a carry-select evaluator circuit.

1 29. The method of claim 27 further comprising:
2 determining a final binary result of adding the
3 first and second binary numbers by utilizing a plurality of
4 carry evaluating circuits in a parallel prefix structure to
5 generate a full set of carry bits from the first binary
6 number and the second binary number.

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